to a pass gate 264. Another pass gate 266 receives the output of a latch 270 that stores the most significant row address bit RA11 responsive to an activate command. The pass gates 264, 266 are controlled by the active low density control signal HD* directly and through an inverter 274. When the HD* signal is inactive high indicative of the full density mode of operation, the pass gate 264 is enabled and the pass gate 266 is disabled so that the latched most significant column address bit CA9 is applied to the column decoder 56 along with the lower order column address bits CA0-CA8. Thus, in the full density mode, the column address buffers 34 operate in a conventional manner. When the HD* signal is active low indicative of the half density mode of operation, the pass gate 264 is disabled and the pass gate 266 is enabled so that the most significant row address bit RA11 is applied by the pass gate 266. As is well known in the art, the row addresses are received prior to the column addresses, and they are latched into the SDRAM 20 responsive to the activate command. In the column address buffers 34 showed in Figure 4, the most significant row address bit RA0 is stored in the latch 270 responsive to the activate command and is then selected by the pass gate 266 for use as the most significant column address bit CA9. In this manner, the most significant row address bit RA11 is remapped to be the most significant column address bit CA9 thereby making the SDRAM 20 with a capacity of M/2 rows * N columns plug compatible with SDRAMs adapted to receive row addresses for M rows and column addresses for N/2 columns.

In the Claims:

Please amend claims 31, 40 and 44 as follows:

31. (Amended) The dynamic random access memory of claim 30 wherein the selector comprises:

a first pass gate coupled between an output of the column address latch and an address output terminal;

a second pass gate coupled between an output of the remapping latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

40. (Amended) The computer system of claim 39 wherein the selector comprises:

a first pass gate coupled between an output of the column address latch and an address output terminal;

a second pass gate coupled between an output of the remapping latch and the address output terminal; and

a control circuit for enabling the first pass gate and disabling the second pass gate or disabling the first pass gate and enabling the second pass gate.

44. (Amended) A method of addressing a dynamic random access memory ("DRAM") having a full density operating mode and a reduced density operating mode, the method comprising:

determining the operating mode of the DRAM;

storing a specific row address bit responsive to a row address strobe signal;

storing a first set of column address bits and a specific column address bit responsive to a column address strobe signal; and

in the full density operating mode, selecting the first set of column address bits and the specific column address bit that were stored responsive to the column address strobe signal;

in the reduced density operating mode, selecting the first set of column address bits that were stored responsive to the column address strobe signal and the specific row address bit that was stored responsive to the row address strobe signal; and

addressing a column of the DRAM using the selected address bits.

In the Abstract:

Please replace the abstract on page 40 with the following:

A dual mode, full density/half density SDRAM includes a refresh controller specifically adapted to refresh memory cells of the SDRAM in the half density mode at a rate that is significantly slower than the rate at which the memory cells are refreshed in the full density mode. In the half density mode, the refresh controller increments a counter at a rate that is half the rate the counter is incremented in the full density mode. A refresh trigger pulse, which